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TRANSMITTAL FORM

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Application No.	10/041,848
Filing Date	October 24, 2001
First Named Inventor	Dean Warren
Art Unit	2112
Examiner Name	Paul R. Myers
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ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Response
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  - [ ] Affidavits/declaration(s)
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- Response to Non-Comply Appeal Brief
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Signature	Paul A Mendonsa
Date	August 1, 2005

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Typed or printed name	**Gayle Bekish**		
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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($)

Complete if Known	
Application Number	10/041,848
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☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($)

SUBMITTED BY *Complete (if applicable)*

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Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Dean WARREN

Serial No.:	10/041,848	Group Art Unit:	2112
Filed:	October 24, 2001	Examiner:	P. Myers

FOR: PIPELINED, UNIVERSAL SERIAL BUS PARALLEL FRAME DELINEATOR AND NRZI DECODER

APPEAL BRIEF

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

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Sir:

In response to the Notice mailed on July 12, 2005, applicant submits this corrected appeal brief, thus perfecting the notice of appeal filed on March 2, 2005. The Summary of claimed subject matter has been updated to include a concise explanation for each independent claim.

The required headings and subject matter follow.

(i) ***Real party in interest.***

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) ***Related appeals and interferences.***

There are no known related appeals and / or interferences.

(iii) ***Status of claims.***

Claims 1-19 are pending in the case, claims 1-13 and 15-19 stand rejected. The rejections of claims 1-13 and 15-19 are being appealed.

(iv) ***Status of amendments.***

No amendments have been made to the originally filed claims. The attached Claims appendix reflects the current status of the claims.

(v) ***Summary of claimed subject matter.***

With reference to claim 1, some embodiments of the invention relate to an integrated circuit including a parallel frame delineation module (e.g. module 302 in Fig. 3, see page 5, lines 16-24) having a plurality of concurrent comparators (e.g. concurrent comparators 602 in Fig. 6, see page 7, lines 16-31) to delineate received frame boundaries within a Universal Serial Bus (USB) peripheral non-return to zero invert (NRZI) data stream (e.g. see Figs. 7-10 and related description on pages 8-10), and an NRZI decoder module (eg. module 304 in Fig. 3, see page 5, lines 16-24) to decode received NRZI encoded data using parallel data processing (e.g. see Fig. 15 and related description on page 12).

With reference to claim 7, some embodiments of the invention relate to an apparatus including one or more Universal Serial Bus (USB) connectors to couple to a communications channel (e.g. serial communications line 208, see Fig. 2, page 5, lines 12-13) carrying a USB data stream and an application specific integrated circuit (e.g. ASIC 200, see Fig. 2, page 5, lines 9-10) comprising a USB transceiver (e.g. USB transceiver 202, see Fig. 2, page 5, line 14), a serial interface engine (e.g. serial interface engine 204, Fig. 2, page 5, lines 14-15) and apparatus-specific logic (e.g. device specific logic 206, Fig. 2, page 5, .line 15), the USB transceiver having concurrent comparators (e.g. concurrent comparators 602 in Fig. 6, see page 7, lines 16-31) to delineate received asynchronous frame boundaries within the USB data stream (e.g. see Figs. 7-10 and related description on pages 8-10) and parallel logic to decode received encoded data (e.g. see Fig. 15 and related description on page 12).

With reference to claim 10, some embodiments of the invention involve a method of delineating asynchronous frame boundaries in a Universal Serial Bus (USB) data stream, the method including receiving a USB data stream (e.g. see Fig. 4, page 5, line 31

– page 6, line 2), searching for a frame delineation marker in the data received using concurrent comparators(e.g. see Fig. 4, page 6, lines 3-5, see also Fig. 6 and related description on pages 7-10), asserting a flag upon detection of the frame delineation marker (see Fig. 6, page 7, lines 28-31), and creating a vector indicating a location of a frame boundary in the data stream (see Fig. 6, page 7, lines 24-26, see also Fig. 8 and related description on page 9).

With reference to claim 17, some embodiments of the invention relate to an integrated circuit including a three-stage pipeline (e.g. three-stage pipeline 404, see Fig. 4, page 5, line 27) to receive consecutive nine-bit fields of data from an incoming Universal Serial Bus (USB) data stream (e.g. see Fig. 4, page 5, line 31 – page 6, line 2), and a parallel start-of-packet detector (e.g. parallel start of packet detector 406, see Fig. 4, page 5, line 28) having concurrent comparators to identify a frame delineation marker in the incoming USB data stream (e.g. see Fig. 4, page 6, lines 3-5).

(vi) ***Grounds of rejection to be reviewed on appeal.***

I. Claims 1-6, 10-11, and 15-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,081,654 (Stephenson) in view of U.S. Pat. No. 6,707,396 (Govindaraman).

II. Claims 7-9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of U.S. Pat. No. 5,884,086 (Amoni).

III. Claims 12-13 and 17-19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of Govindaraman and further in view of U.S. Pat. No. 6,041,430 (Yamauchi).

(vii) ***Argument.***

I. The rejection of claims 1-6, 10-11, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,081,654 (Stephenson) in view of U.S. Pat. No. 6,707,396 (Govindaraman) is in error and should be reversed.

Claim 1

With respect to claim 1, the rejection of record states that "Govindaraman teaches the use of a NRZI decoder module to decode received USB NRZI data using parallel processing." See final office action, page 5, lines 3-4. The Examiner has now admitted that this is incorrect: "In regards to applicants arguments that Govindaraman teaches the sync detect being in a serial stream: The examiner agrees." See final office action, page 2, lines 15-16. As previously noted by the applicants, the NRZI decoder 240 is likewise in the serial stream. Accordingly, the Examiner has admitted that the rejection of record is in error because the NRZI decoder 240 of Govindaraman does not use parallel processing.

Applicants do not understand why the Examiner did not withdraw the rejection, or at least re-state or re-formulate the rejection. But as it stands, the rejection of record is admittedly erroneous and should be reversed. Although applicants believe that the Board should reverse the rejection of claim 1 for the substantive reasons set forth herein, at a minimum the Board should remand the case and require the Examiner to properly articulate the rejection of record.

Moreover, with respect to claim 1, the rejection is internally inconsistent. The rejection identifies Stephenson as the primary reference and alleges that Stephenson teaches various claim recitations including (paraphrasing from the final office action):

- an integrated circuit;
- a parallel frame delineation module (20);
- a plurality of concurrent comparators (32, 34);

- to delineate received frame boundaries (abstract);
- within a data stream (22).

The rejection then admits that Stephenson (the primary reference) lacks the NRZI decoder module to decode received USB NRZI using parallel data processing and appears to rely on Govindaraman (the secondary reference) to provide the missing teaching (now admitted to be erroneous). However, the rejection then proposes to modify the secondary reference (Govindaraman) with some unidentified sync detect from the primary reference (Stephenson). The proposed modification is internally inconsistent with the remainder of the rejection and fails to establish how Govindaraman, after the proposed modification, would teach or suggest all of the claim recitations (which are otherwise alleged to be contained in Stephenson, not in Govindaraman).

Applicants requested clarification of the Examiner's position and in the Examiner's Response to Arguments the Examiner cites the title, the abstract, every figure, and every column of Stephenson. See final office action at page 2, lines 8-10. Applicants fail to understand how this clarifies the Examiner's position or advances the prosecution.

Applicants do not understand why the Examiner did not withdraw the rejection, or at least re-state or re-formulate the rejection. But as it stands, the rejection of record is erroneous and should be reversed. Although applicants believe that the Board should reverse the rejection of claim 1 for the substantive reasons set forth herein, at a minimum the Board should remand the case and require the Examiner to properly articulate the rejection of record.

In any event, the rejection of record fails to establish even a prima facie case of obviousness. Claim 1 recites, among other things, an NRZI decoder module to decode received NRZI encoded data using parallel data processing. The final office action admits that "Stephenson does not teach the ... NRZI decoder using parallel processing." See final office action at page 5, lines 1-3. The Examiner now agrees that the

components along data path 110 in Govindaraman are serial components (at least until the serial to parallel converter 260), including the sync detect 230, the NRZI decoder 240, and the bit un-stuffer 250. Accordingly, Govindaraman also fails to teach or suggest the recited NRZI decoder module to decode received NRZI encoded data using parallel data processing. Because neither reference teaches or suggests, among other things, the recited NRZI decoder module to decode received NRZI encoded data using parallel data processing, the rejection of record fails to establish a prima facie case of obviousness and no combination of the references can possibly teach or suggest all of the claim recitations of claim 1.

Applicants note that applicants are not arguing the references individually, but rather are arguing that any proposed combination still fails to establish a prima facie case of obviousness. As noted in MPEP § 706.02(j), one of the requirements to establish a prima facie case of obviousness is that the prior art references must teach or suggest all of the claim recitations. Where a claim feature is absent from each individual reference, no combination of the references can establish a prima facie case of obviousness. Assuming for the sake of argument, that the sync detect 230 of Govindaraman was replaced with some as yet unidentified sync detect from Stephenson, the resulting circuit would still lack the recited NRZI decoder module to decode received NRZI encoded data using parallel data processing.

Finally, with respect to claim 1, the Examiner provides only a contrived motivation to modify Govindaraman with the teachings of Stephenson, namely "because this would have for the handling of high speed data streams in parallel." In fact, Govindaraman handles high speed data streams already ("for example, 480 Mbit/sec used in USB 2.0 devices", see col. 2, lines 59-60). Moreover, Govindaraman teaches that the sync detector 230 operates at a lower local clock rate for parallel processing. See Govindaraman, col. 2, lines 55-62. No one of ordinary skill in the art would find it necessary or desirable to modify the state of the art circuit disclosed in Govindaraman (which can already handle "high speed data streams" in serial and/or parallel) with the fifteen year old technology described in Stephenson.

Although not well articulated, the Examiner appears to be suggesting that Govindaraman be modified to use the parallel frame synchronization circuit 20 of Stephenson instead of the sync detect circuit 230. However, this combination is unworkable and has no reasonable expectation of success. Applicant note that the circuit 20 includes a serial to parallel converter 24 so that, in the proposed modification, data provided to the admittedly serial NRZI decoder 240, serial bit un-stuffer 250, and later serial to parallel converter 260 would be indecipherable. It is clear that substantial further modification to the circuit 100 would be required to arrive at any type of workable system.

In the Examiner's response to applicants' arguments at page 2, although not well articulated, the Examiner appears to be suggesting that Stephenson provides motivation to modify Govindaraman's entire system to be a parallel system. Again applicants note that this appears to be an unworkable modification which would change a fundamental operating principle of the modified reference. For example, the down stream serial bit un-stuffer 250 would become inoperable. Also, the downstream serial to parallel converter 260 would become inoperable and superfluous.

Because the rejection of record in the final office action is facially erroneous and internally inconsistent, and because the office action fails to establish a prima facie case of obviousness, and because the proposed motivation to combine the references is erroneous, and because the proposed modification is unworkable, claim 1 is patentable over any combination of Stephenson and Govindaraman. Claims 2-6 depend either directly or indirectly from claim 1 and are likewise patentable.

Claim 5

With respect to claim 5, applicants provide the following side-by-side comparison for the Board's convenience:

Claim 5:	Rejection of claim 5:	Column 1 lines 20-26
5. The integrated circuit of claim 3, wherein the parallel frame boundary delineation module further comprises a parallel start-of-packet detector.	In regards to claim 5: Stephenson teaches detecting the start of frame by matching a framing pattern (Column 1 lines 20-26).	Generally frame synchronization of an incoming serial bit data stream is performed by comparing a known framing pattern to the incoming data which contains periodic frame synchronization information so as to determine the frame boundary (start of frame) based upon matching the frame synchronization information to the framing pattern.

The rejection of claim 5 is not understood because the language cited in the office action does not correspond to the claim language and the cited portion of the reference does not appear to read on the claim language. Clarification was respectfully requested, but no clarification was provided. The Examiner has yet to communicate any proper basis for the rejection of claim 5, thus depriving the applicants of a fair opportunity to reply, contrary to the requirements of MPEP § 706.02(j). Although applicants believe that the Board should reverse the rejection of claim 5 for the substantive reasons set forth herein, at a minimum the Board should remand the case and require the Examiner to properly articulate the rejection of record.

Applicants do not know if the rejection is simply a typographical or editorial error, or if the Examiner is actually asserting that the cited portion of col. 1, lines 20-26 reads on claim 5. Applicants notes that the cited portion appears to relate only to serial operations, and not to any parallel start-of-packet detector. Applicants cannot further respond to a rejection of claim 5 which has not been clearly explained by the Examiner, contrary to the requirements of MPEP § 706.02(j) and MPEP § 707.07(f), other than to

note that by failing to identify how the cited portion reads on the claim recitations the Examiner has failed to establish a prima facie case of obviousness.

Claim 10

With respect to claim 10, the rejection of record completely fails to address the recitations of claim 10. Claim 10 is a method claim having a different scope as compared to claim 1. For example, the office completely fails to mention any recitations of claim 10 including at least: asserting a flag upon detection of the frame delineation marker; and creating a vector indicating a location of a frame boundary in the data stream. Applicants submit that neither of the cited references, alone or in combination, teach or suggest asserting a flag upon detection of the frame delineation marker; and creating a vector indicating a location of a frame boundary in the data stream. Accordingly, claim 10 and its dependent claims 11-16 are believed to be patentable.

In the Examiner's Response to Arguments, the Examiner asserts that the office action addresses the recitations of claim 10 on page 2. Claim 10 recites, among other things:

> searching for a frame delineation marker in the data received using concurrent comparators;
>
> asserting a flag upon detection of the frame delineation marker; and
>
> creating a vector indicating a location of a frame boundary in the data stream.

Applicants have thoroughly reviewed page 2 of the prior office action and cannot find any of the following terms from the foregoing recitations: searching, marker, asserting, flag, creating, vector, indicating, or location. The rejection of record is sorely deficient and should be withdrawn.

Applicants further note that the Examiner's comments in the Response to Arguments form no part of the rejection of record. Assuming, for the sake of argument, that the

Board would give any weight to such comments, applicants note that the comments fall far short of meeting the requirements under MPEP § 706.02(j) for the contents of a 35 U.S.C. § 103 rejection. Although applicants believe that the Board should reverse the rejection of claim 10 for the substantive reasons set forth herein, at a minimum the Board should remand the case and require the Examiner to properly articulate the rejection of record.

In order to expedite the prosecution, applicants further note that the terms 'flag' and 'vector' cannot be located anywhere in either the Stephenson or the Govindaraman references. Applicants further note that the output signal 42 is not a flag and does not appear to asserted upon detection of any frame delineation marker. Applicants further note that 'F6' and '28' are not vectors and, if they were, they are not vectors indicating the location of the frame boundary in the data stream (they are at most markers in the data stream).

Because the rejection of record fails to identify how the recitations of claim 10 are allegedly taught or suggested by the references, the Examiner has failed to establish a prima facie case of obviousness and claim 10 is patentable over the cited references.

Claim 16

With respect to claim 16, the claim recites that the vector created comprises an eleven-bit vector. Applicants maintain that the relied upon 16 output bits of comparators 32 and 34 do not relate to the recited eleven-bit vector. In fact, the output of comparators 32 and 34 do not relate to any vector indicating a location of a frame boundary in the data stream.

II. The rejection of claims 7-9 under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of U.S. Pat. No. 5,884,086 (Amoni) is in error and should be reversed.

In the Examiner's response to applicants' arguments, the Examiner for the first time cites a new reference (the USB 1.0 specification) and communicates the basis for reliance on the contents of that reference, but without positively including the reference in the rejection, contrary to the requirements of MPEP § 706.02(j). MPEP § 706.02(j) sets forth that "[w]here a reference is relied on to support a rejection, whether or not in a minor capacity, that reference should be positively included in the statement of the rejection. See *In re Hoch,* 428 F.2d 1341, 1342 n.3 166 USPQ 406, 407 n. 3 (CCPA 1970)." Although applicants believe that the Board should reverse the rejection of claims 7-9 for the substantive reasons set forth herein, at a minimum the Board should remand the case and require the Examiner to properly articulate the rejection of record.

Claim 7 recites one or more Universal Serial Bus (USB) connectors to couple to a communications channel carrying a USB data stream; an application specific integrated circuit comprising a USB transceiver, a serial interface engine and apparatus-specific logic, the USB transceiver having concurrent comparators to delineate received asynchronous frame boundaries within the USB data stream and parallel logic to decode received encoded data. The rejection of record asserts, without support or citation to any text portion or drawings element, that Amoni discloses a USB transceiver, a serial interface engine, and apparatus specific logic. In fact, Amoni makes no reference to such elements. Accordingly, the rejection of record fails to establish a prima facie case of obviousness. Amoni is related to providing power to USB 1.0 peripherals and does not discuss the transceiver / serial interface aspects of the USB devices.

In any event, the rejection of record provides only a contrived motivation to combine the references. The rejection of record proposes to modify Amoni with the teachings of Stephenson 'because this would have for the handling of high speed data

streams in parallel." Amoni, as noted above, is concerned with power delivery to USB 1.0 devices, and has no need for handling high speed data streams in parallel. As explicitly stated several times in Amoni, the top supported speed is 12 Mbits. In fact, Stephenson teaches away from the combination. Stephenson clearly states that the circuit disclosed therein is useful for data streams above 50 MHz (see col. 1, lines 27-34, col. 2, lines 32-40, and col. 5, line 66 - col. 6, line 3). Absent the hindsight afforded by the present specification, one of ordinary skill in the art would not be motivated to modify Amoni with the circuit of Stephenson because Stephenson's circuit is simply not necessary for handling a 12 Mbit data stream.

In any event, the rejection of record fails to establish even a prima facie case of obviousness. Claim 7 recites, among other things, parallel logic to decode received encoded data. The office action admits in connection with claim 1 that Stephenson fails to teach NRZI decoding. In fact, Stephenson does not teach anything whatsoever with respect to decoding encoded data, parallel or otherwise. The data stream in Stephenson is simply not encoded. The rejection of record does not cite any portion of Amoni for this missing teaching.

Applicants further note that the Examiner's comments in the Response to Arguments form no part of the rejection of record. Assuming, for the sake of argument, that the Board would give any weight to such comments, applicants note that the Examiner erroneously states that "Stephenson teaches parallel decoding done by any of the multiple detectors as well as handling the data in parallel." Applicants note that the Examiner provides no citation to any supporting portion of Stephenson for this alleged teaching, and in fact the words 'decode' or 'decoding' do not appear in Stephenson. At best, Stephenson describes some parallel handling of data, but not the recited parallel logic to decode received encoded data.

Applicants note that applicants are not arguing the references individually, but rather are arguing that any proposed combination still fails to establish a prima facie case of obviousness. As noted in MPEP § 706.02(j), one of the requirements to establish a

prima facie case of obviousness is that the prior art references must teach or suggest all of the claim recitations. Where a claim feature is absent from each individual reference, no combination of the references can establish a prima facie case of obviousness. Assuming for the sake of argument, that Amoni was somehow modified as proposed to use the 'start of frame detect' from Stephenson, the resulting circuit would still lack the recited parallel logic to decode received encoded data.

Because the rejection of record fails to establish a prima facie case of obviousness and because the proposed motivation to combine the references is erroneous, claim 7 is patentable over Stephenson in view of Amoni. Dependent claims 8 and 9 are likewise patentable.

Claim 9

Applicants note that claim 9 further recites that the parallel logic decodes non-return to zero invert (NRZI) encoded data, which was admitted as being absent from the techings of Stephenson. Specifically, on page 2 of the final office action the Examiner admits "Stephenson does not teach the parallel frame delineation being in a USB peripheral NRZI data stream including NRZI decoder using parallel data processing." Although Amoni mentions NRZI, Amoni does not teach or suggest parallel logic to decode NRZI encoded data. The Examiner's further citation to the USB Spec fails to overcome this deficiency in both Stephenson and Amoni.

The Examiner disingenuously attempts to cure some of the above deficiencies essentially by making new grounds of rejection in the Examiner's Response to Arguments. Applicants note that the Examiner's comments in the Response to Arguments form no part of the rejection of record. Assuming, for the sake of argument, that the Board would give any weight to such comments, applicants note that in several instances the Examiner relies on citations to the newly cited USB Spec which is not of record in the rejection. By doing so, the Examiner has implicitly admitted that the rejection of record is deficient. Applicants do not understand why the Examiner did not

withdraw the rejection, or at least re-state or re-formulate the rejection. But as it stands, the rejection of record is admittedly erroneous and should be reversed.

In order to expedite the prosecution of the application, applicants further stress that none of the cited references, namely Stephenson, Amoni, or the USB 1.0 Spec, teaches or suggests the recited parallel logic to decode received NRZI encoded data. Applicants again note that applicants are not arguing the references individually, but rather are arguing that any proposed combination still fails to establish a prima facie case of obviousness. As noted in MPEP § 706.02(j), one of the requirements to establish a prima facie case of obviousness is that the prior art references must teach or suggest all of the claim recitations. Where a claim feature is absent from each individual reference, no combination of the references can establish a prima facie case of obviousness. Assuming for the sake of argument, that Amoni was somehow as proposed (even including the teachings of the USB Spec), the resulting circuit would still lack the recited parallel logic to decode received NRZI encoded data.

III. The rejection of claims 12-13 and 17-19 under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of Govindaraman and further in view of U.S. Pat. No. 6,041,430 (Yamauchi) is in error and should be reversed.

With respect to claims 12-13, these claims depend either directly or indirectly from patentable claim 10, and are also believed to be patentable. Yamauchi, which is relied upon for elements of claims 12 and 13, fails to make up for the deficiencies in the other references with respect to claim 10.

Claims 12-13 and 17-19

Yamauchi is non-analogous art with respect to the other cited references. Both Stephenson and Govindaraman relate to serial bit streams, while Yamauchi relates to parallel communication between internal components. Applicants note that the classifications of the references are dissimilar.

The Examiner's motivation to combine is completely contrived and does not have any basis in the references. Moreover, the Examiner fails to consider how Stephenson teaches away from the proposed modification. Applicants first note that Stephenson is directed to a high speed serial bit stream. Adding an extra parity bit every ninth bit in the serial data stream would represent a high performance penalty. Accordingly, one of ordinary skill in the art would not be motivated to modify Stephenson as proposed with the teachings of Yamauchi to add a nine parity bit in the data stream. Moreover, Stephenson relates to the SONET standard (see col. 4, lines 56-59), which does not provide for the proposed ninth parity bit and likely provides its own error correction scheme. One of ordinary skill in the art would not be motivated to modify Stephenson with the proposed parity bit every ninth bit because such modification would make Stephenson unworkable for its original purpose of supporting the SONET standard.

Claim 12

Moreover, the Examiner misconstrues the claims and the reference as it might be applied to the claims. Claim 12 recites NRZI data is received in nine-bit fields. The ninth parity bit does not correspond to a data bit, so modifying Stephenson with the proposed parity bit still results in only an 8 bit data field. Moreover, adding a parity bit to every ninth bit location of NRZI encoded data would likely conflict with the NRZI encoding scheme and defeat the purpose of using NRZI data.

Claim 13

Claim 13 recites that the act of searching for a frame delineation marker is performed concurrently on a twenty-seven bit field of data. Applicants first note that the proposed parity bit would not be considered a data bit, and so modifying Stephensen as proposed still results in a 24 bit data field. Alternatively, interposing an arbitrary parity bit every ninth bit would conflict with the decoding of the frame delineation marker in Stephenson.

Claim 17

For the reasons given above, Yamauchi is non-analogous art and the proposed modification is unfounded and unworkable. Moreover, for at least the reasons given above with respect to claim 1, the office action fails to establish motivation to combine Stephenson and Govindaraman, and further because the proposed modification is unworkable, claim 17 is patentable over the combination of Stephenson, Govindaraman, and Yamauchi. Claims 18-19 depend either directly or indirectly from claim 17 and are likewise patentable.

Claim 17 recites a three-stage pipeline to receive consecutive nine-bit fields of data from an incoming Universal Serial Bus (USB) data stream. The ninth parity bit does not correspond to a data bit, so modifying Stephenson with the proposed parity bit still results in only an 8 bit data field. Moreover, one of ordinary skill in the art would not be motivated to add a parity bit every ninth bit position in a USB data stream, because the performance penalty is too high.

Claim 18

The rejection of record states "Stephenson teaches NRZI." However, this is in direct contradiction to several admissions of the Examiner, including "[w]hat Stephenson fails to teach is NRZI decoding." (see page 4, lines 7-8 of the final office action). Although applicants believe that the Board should reverse the rejection of claim 18 for the substantive reasons set forth herein, at a minimum the Board should remand the case and require the Examiner to properly articulate the rejection of record.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

August 1, 2005
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(viii) ***Claims appendix.***

1. An integrated circuit comprising:

a parallel frame delineation module having a plurality of concurrent comparators to delineate received frame boundaries within a Universal Serial Bus (USB) peripheral non-return to zero invert (NRZI) data stream; and

an NRZI decoder module to decode received NRZI encoded data using parallel data processing.

2. The integrated circuit of claim 1, wherein the USB peripheral NRZI data stream follows a protocol defined in version 2.0 of the USB specification.

3. The integrated circuit of claim 2, wherein the parallel frame boundary delineation module comprises a three-stage pipeline.

4. The integrated circuit of claim 3, further comprising a pipeline control state machine.

5. The integrated circuit of claim 3, wherein the parallel frame boundary delineation module further comprises a parallel start-of-packet detector.

6. The integrated circuit of claim 5 wherein the parallel start-of-packet detector comprises eleven concurrent comparators.

7. An apparatus comprising:

one or more Universal Serial Bus (USB) connectors to couple to a communications channel carrying a USB data stream;

an application specific integrated circuit comprising a USB transceiver, a serial interface engine and apparatus-specific logic, the USB transceiver having concurrent comparators to delineate received asynchronous frame boundaries within the USB data stream and parallel logic to decode received encoded data.

8. The apparatus of claim 7, wherein the apparatus-specific logic comprises logic for an apparatus selected from the group consisting of: a hub, a digital camera, a video-conferencing camera, a printer, a keyboard, a scanner, a modem, a digital phone, a removable media drive, a CD/DVD drive, a gaming device, a hard drive, a mouse, a trackball, a pointer, a display device, a speaker and a networking device.

9. The apparatus of claim 7, wherein the parallel logic decodes non-return to zero invert (NRZI) encoded data.

10. A method of delineating asynchronous frame boundaries in a Universal Serial Bus (USB) data stream, the method comprising:

receiving a USB data stream;

searching for a frame delineation marker in the data received using concurrent comparators;

asserting a flag upon detection of the frame delineation marker; and

creating a vector indicating a location of a frame boundary in the data stream.

11. The method of claim 10, wherein the USB data stream comprises non-return to zero invert (NRZI) data.

12. The method of claim 11, wherein the NRZI data is received in nine-bit fields.

13. The method of claim 10, wherein the act of searching for a frame delineation marker is performed concurrently on a twenty-seven bit field of data.

14. The method of claim 13, wherein the frame delineation marker comprises "00101010".

15. The method of claim 10, wherein the act of searching is performed by eleven concurrent comparators.

16. The method of claim 10, wherein the vector created comprises an eleven-bit vector.

17. An integrated circuit comprising:

a three-stage pipeline to receive consecutive nine-bit fields of data from an incoming Universal Serial Bus (USB) data stream; and

a parallel start-of-packet detector having concurrent comparators to identify a frame delineation marker in the incoming USB data stream.

18. The integrated circuit of claim 17, further comprising a non-return to zero invert (NRZI) data decoder to decode the incoming USB data stream.

19. The integrated circuit of claim 18, further comprising a state machine to determine when the incoming USB data stream contains valid data.

(ix) ***Evidence appendix.***

None.

(x) ***Related proceedings appendix.***

None.